ChipXpert

THINK. DESIGN. OPTIMIZE

Advanced Analog Layout

Turn Circuits into Silicon – Become an Analog Layout Engineer

Offline/Online Mode

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www.chipxpert.in

Madhapur ,Hyderabad, Telangana

About us

ChipXpert VLSI Training Institute is a premier institution dedicated to providing state-of-the-art training in Very-Large-Scale Integration (VLSI) design and semiconductor technology. With our commitment to bridging the gap between academic knowledge and industry requirements, we ensure aspiring engineers are fully prepared for successful careers in the fast-paced semiconductor and electronics industry. Our programs are designed by industry veterans, integrating theoretical foundations with practical expertise.

Eligibility Criteria

- B.Tech/B.E final-year students (ECE/EEE/Instrumentation).
- M.Tech/M.Sc 1st/2nd-year students (VLSI/Embeded).
- Graduates with completed B.Tech/M.Tech degrees.

Modes of Training Offered

- Classroom-Based Offline Training
- Interactive Online Training Sessions
- Industry-Focused Internship Program

Unique Features

- Guaranteed 100% Placement Assistance
- Impressive Hands-On 24/7 Labs & Projects
- Curriculum with Latest Industry Tools
- Corporate-Level Professional Training
- Flexible Training Modes with 24/7 eLearn Access
- Expert Trainers and Guest Sessions

Learning Outcome

- Perform floorplanning and plan power/ground routing for analog/mixed-signal blocks.
- Apply matching techniques such as common centroid and interdigitated layout.
- Implement shielding, guard rings, and substrate isolation to ensure noise immunity.
- Handle parasitics, IR drop, and layout-dependent effects (LDE) in deep-submicron nodes.
- Run and debug DRC/LVS/ERC checks as part of physical verification.
- Perform parasitic extraction (PEX) and support post-layout simulation.

Trainers Details

- 15+ years of industry experience in Analog Layout Design, working with leading semiconductor companies such as Texas Instruments, STMicroelectronics, Intel, and NXP.
- Expertise in full-custom layout of analog/mixed-signal blocks including Op-Amps, Bandgap References, PLLs, ADCs, DACs, and High-Speed IOs.
- Proven experience across advanced technology nodes (28nm, 16nm, 7nm, and below) with successful tape-outs of high-performance analog IPs.
- Strong command over matching techniques, parasitic-aware layout, shielding, guard rings, and electromigration compliance.
- Hands-on knowledge of layout verification flows including DRC, LVS, ERC, and Antenna Checks using industry-standard sign-off tools.
- Skilled in Cadence Virtuoso, Calibre, Assura, and other custom layout EDA tools aligned with current foundry requirements.
- Track record of training and mentoring engineers in deep-submicron layout practices with a focus on layout productivity and quality.

Analog Layout Design Overview

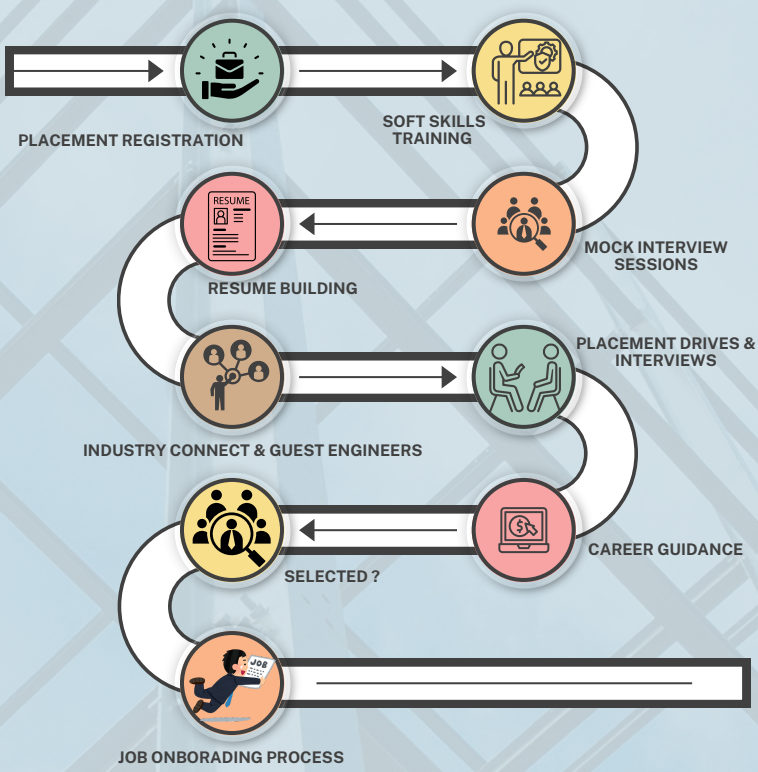
The Advanced Analog Layout Design Course by ChipXpert is designed for students and professionals aiming to build a strong career in custom analog and mixed-signal layout. Curated by experienced layout engineers from companies like Texas Instruments, Intel, and STMicroelectronics, the course provides end-to-end training on analog layout methodologies and industry-standard practices.

The program covers layout design of critical analog blocks such as Op-Amps, Bandgap References, ADCs, DACs, and PLLs, with a strong focus on matching techniques, parasitic-aware layout, floorplanning, and layout optimization. It also includes comprehensive training on DRC, LVS, and ERC checks, along with deep-submicron challenges at nodes like 14nm,28nm, 16nm, and below.

COURSE CURRICULUM

S.No	Module Topic	Module Description
1	Introduction to Analog Layout	Basics of analog layout design, key differences from digital layout, design hierarchy, layout flow, and understanding schematic-to-layout mapping.
2	CMOS Devices and Layout Rules	Layout of MOS transistors, wells, diffusion, poly, metal layers, design rules (DRC), L:W ratio, and matching techniques.
3	Layout of Passive Devices	Layout techniques for resistors, capacitors, and diodes, including dummy structures, shielding, and parasitic minimization.
4	Common Layout Topologies	Techniques like common centroid, interdigitated layout, symmetrical placement, and routing strategies for analog precision.
5	Parasitics and Layout-Dependent Effects	Understanding parasitic capacitance/resistance, IR drop, LDE (layout-dependent effects), and their impact on performance.
6	Floorplanning and Area Optimization	Floorplanning strategies for analog blocks, power/ground routing, aspect ratio control, and area estimation methods.
7	Guard Rings and Shielding	Implementation of guard rings, substrate isolation, shielding strategies to prevent noise coupling and improve reliability.
8	LVS and DRC Checks	Introduction to physical verification, running and fixing DRC (Design Rule Check), LVS (Layout vs Schematic), and interpretation of errors.
9	Advanced Layout Topics	Techniques for high-speed analog layout, RF layout considerations, and deep submicron challenges in 28nm, 16nm, and below.
10	Analog IP Block Layout	Hands-on layout for Op-Amps, Bandgap references, ADC/DAC sub-blocks, and layout planning for analog IP.
11	ESD and IO Cell Layout	ESD and IO Cell Layout ESD protection layout design, IO cell planning, ESD rule checks, and strategies for robust pad-ring design.
12	Capstone Project & Final Evaluation	Full-cycle analog layout project from schematic to tapeout with DRC/LVS closure. Final evaluation based on review, metrics, and documentation.

Placement Process



MOCK INTERVIEWS WITH INDUSTRY EXPERTS

REAL-TME INDUSTRIAL PROJECT

COURSE COMPLETION CERTIFICATE

100+ Hiring Companies

Actel, Advanced Linear Devices, Inc., Agilent Technologies, AKM, Allegro, ALi, Altera, AMD, Analog Devices, Atmel, austriamicrosystems, Broadcom, Cirrus Logic, Conexant, Cypress, Exar, Fairchild Semiconductor, Halo Electronics, Inc., Holtek, hynix, intel, intersil, Hitachi, IDT, Infineon, International Rectifier, ISSI, KEC, level one, Lansdale Semiconductor Inc., Littelfuse, Linear Technology, MXIC, Marvell, maxim integrated, Micrel, Microlinear, Micron, Microchip, Micronas, Microsemi, molex, Motorola, National Semiconductor, NXP, OmniVision, Omron, ON Semiconductor, PLX Technology, Pericom, Phoenix Contact, PMC, Qualcomm Incorporated

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