ASIC Design Verification

Build a verification foundation in SystemVerilog and UVM, including testbench architecture, assertions, coverage and debug.

What you will study

01	**Foundations** Electronics and CMOS; digital logic; UNIX/Linux; ASIC flow; Verilog; DFT, Tcl, synthesis and STA introductions.
02	**SystemVerilog** Data types, classes and object-oriented concepts; interfaces; randomization; functional coverage; assertions.
03	**UVM fundamentals** Simulation phases; factory and configuration; agents, drivers, monitors, scoreboards, sequences and sequence items.
04	**UVM advanced** TLM; ports and FIFOs; callbacks; factory overrides; virtual sequences; register models.
05	**Debug and coverage** Simulator and waveform debugging; coverage planning, analysis and closure.
06	**Practice and review** Verification project examples using interfaces such as AXI or UART; testbench review and debug.

Batch and learning format

For confirmed start dates, visit the live batch calendar. Online and Hyderabad/Bengaluru classroom options are advertised. Ask admissions to confirm the timetable, seat availability, fees and current lab access for your chosen batch.

Explore the current course page

https://chipxpert.in/asic-design-verification-course/

For admissions: +91 83098 18310 | chipxpert.in/contact/