ChipXpert

THINK. DESIGN. OPTIMIZE

Advanced Physical Design

Turn Circuits into Silicon –
Become a Physical Design Engineer

www.chipxpert.in

About us

ChipXpert VLSI Training Institute is a premier institution dedicated to providing state-of-the-art training in Very-Large-Scale Integration (VLSI) design and semiconductor technology. With our commitment to bridging the gap between academic knowledge and industry requirements, we ensure aspiring engineers are fully prepared for successful careers in the fast-paced semiconductor and electronics industry. Our programs are designed by industry veterans, integrating theoretical foundations with practical expertise.

Eligibility Criteria

- B.Tech/B.E final-year students (ECE/EEE/Instrumentation).
- M.Tech/M.Sc 1st/2nd-year students (VLSI/Embeded).
- Graduates with completed B.Tech/M.Tech degrees.

Modes of Training Offered

- Classroom-Based Offline Training
- Interactive Online Training Sessions
- Industry-Focused Internship Program

Unique Features

- Guaranteed 100% Placement Assistance
- Impressive Hands-On 24/7 Labs & Projects
- Curriculum with Latest Industry Tools
- Corporate-Level Professional Training
- Flexible Training Modes with 24/7 eLearn Access
- Expert Trainers and Guest Sessions

Learning Outcome

- Understand RTL to GDSII flow and design stages.
- Perform Floorplanning, Power Planning, and Placement.
- Implement Clock Tree Synthesis (CTS) and Routing.
- Analyze and fix timing violations using STA.
- Apply Low Power Design techniques (UPF/CPF).
- Run DRC/LVS checks and understand Physical Verification.
- Handle ECOs and prepare for Tape-out.
- Gain experience with industry-standard EDA tools.
- Learn and apply TCL scripting for tool automation

Trainers Details

- 15+ years of industry experience in VLSI Physical Design, working with global semiconductor leaders like NVIDIA, Qualcomm, Intel, and AMD.
- Deep expertise in RTL to GDSII flow, including Floorplanning, Power Planning, Placement, CTS, Routing, and Physical Verification.
- Hands-on experience in advanced technology nodes (7nm, 5nm, 3nm) with successful tape-out of multiple complex SoCs.
- Proficient in Static Timing Analysis (STA), Signal Integrity, Clock Tree Optimization, and Timing Closure techniques.
- Strong background in Low Power Design methodologies using UPF/CPF, and handling ECOs in late-stage design.
- Extensive tool knowledge in Cadence, Synopsys, and Mentor Graphics EDA tools, aligned with current industry practices.
- Proven track record of mentoring and training freshers and professionals with a focus on real-time, hands-on learning.
- Training programs are designed to bridge the gap between academia and industry, making students job-ready for VLSI roles.

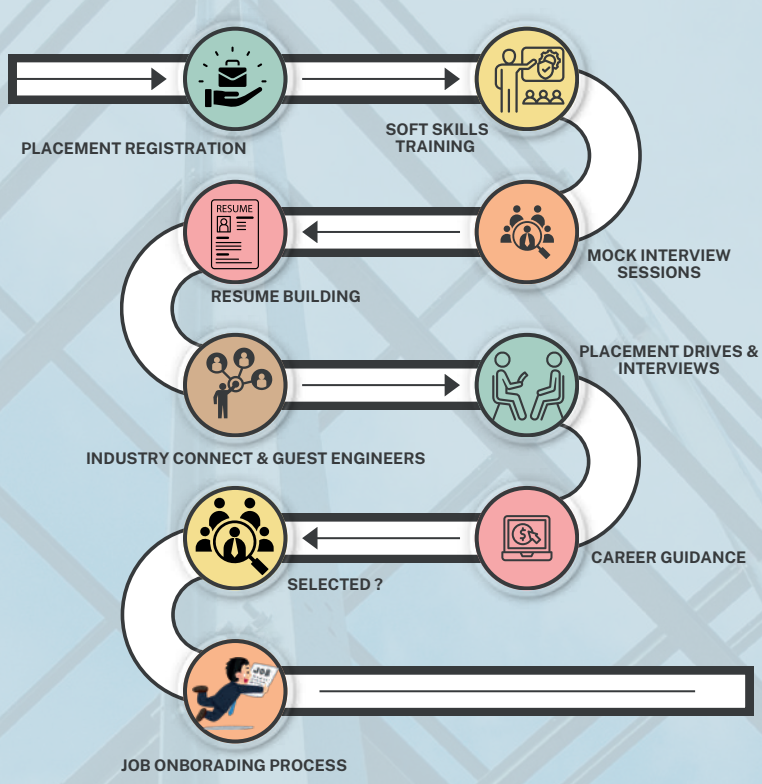
Physical Design Course Overview

ChipXpert proudly introduces its Advanced Physical Design (PD) Course, specially designed for students and professionals aiming to build a strong career in VLSI backend design. This course is curated by industry experts with over 15 years of experience at leading semiconductor companies like NVIDIA, Qualcomm, Intel, and AMD. It offers in-depth training on the complete RTL to GDSII flow, covering advanced topics such as Floorplanning, Power Planning, Placement, Clock Tree Synthesis (CTS), Routing, Static Timing Analysis (STA), Low Power Design using UPF/CPF, Physical Verification (DRC/LVS), and Tape-out preparation. Learners will also gain hands-on experience in TCL scripting for design automation, and real-time exposure to industry-standard EDA tools and interview preparation, We equips learners with job-ready skills to succeed in top VLSI companies.

COURSE CURRICULUM

S.No	Module Name	Sub-Modules
1	Introduction to Electronics, MOSFET & CMOS Theory	- Introduction to Electronics and MOSFET Theory - Introduction to CMOS Process and Circuits
2	Digital Electronics	- Binary System and Boolean Algebra - Combinational Circuits - Sequential Circuits – Counters, State Machines, Shift Registers
3	Basics of UNIX/LINUX	- Introduction to Unix/Linux Commands - VI Editor Commands
4	Introduction to ASIC Design	- ASIC Flow - All Stages Discussion
5	Introduction to Verilog	- Basic Concepts - Gate-Level Modeling - Dataflow Modeling - Behavioural Modeling - Tasks and Functions
6	Introduction to DFT	- DFT Basics - Fault Modeling - Logic and Fault Simulation - SCAN Design - Introduction to BIST
7	TCL Programming	- Introduction to TCL Syntax - Variables and Control Structures - File Operations - Loops and Procedures - TCL in EDA Tools (Synopsys/Cadence) - Scripting Best Practices
8	Synthesis	- Inputs and Outputs Understanding - Constraints Development and Understanding - Optimization Techniques (Unify, Preserve, Flatten) - Wireload Model: PLE, Physical, Spatial
9	Static Timing Analysis	- Transition/Slew, Capacitance, Leakage Power, Internal Power, On-Chip Variation (Derate, AOCV, LVF) - Library File Differences: NLDM, CCS, ECSM, LVF - Setup, Hold, Recovery, Removal, Pulse Width, Clock Gating Check
10	Physical Design Overview	- Overview of Physical Design Stages
11	Physical Design - Step 1: Input and Floorplanning	- Input Files, Sanity Checks, and IO Placement - Floorplanning Concepts
12	Physical Design - Step 2: Power Planning	- Designing Power Grid - IR Drop Estimation - Electromigration Checks
13	Physical Design - Step 3: Placement	- Standard Cell Placement - Placement Optimization - Congestion Analysis
14	Physical Design - Step 4: Clock Tree Synthesis	- Clock Tree Insertion - Skew and Latency Optimization
15	Physical Design - Step 5: Routing	- Global and Detailed Routing - Signal Integrity - Crosstalk Avoidance
16	Physical Design - Step 6: Optimization and ECO	- Post-Route Optimization - ECO Implementation - Timing Closure
17	Physical Design Verification	- Design Rule Checks Understanding and Importance - Layout Versus Schematic and LEC - Electrical Rule Checks - IR Drop Analysis – Static and Dynamic
18	Industry Standard Project Execution	- Industry Standard Physical Design Live Project
19	Mock Interviews & Personality Development	

Placement Process



MOCK INTERVIEWS WITH INDUSTRY EXPERTS

REAL-TME INDUSTRIAL PROJECT

COURSE COMPLETION CERTIFICATE

100+ Hiring Companies

Actel, Advanced Linear Devices, Inc., Agilent Technologies, AKM, Allegro, ALi, Altera, AMD, Analog Devices, Atmel, austriamicrosystems, Broadcom, Cirrus Logic, Conexant, Cypress, Exar, Fairchild Semiconductor, Halo Electronics, Inc., Holtek, hynix, intel, intersil, Hitachi, IDT, Infineon, International Rectifier, ISSI, KEC, level one, Lansdale Semiconductor Inc., Littelfuse, Linear Technology, MXIC, Marvell, maxim integrated, Micrel, Microlinear, Micron, Microchip, Micronas, Microsemi, molex, Motorola, National Semiconductor, NXP, OmniVision, Omron, ON Semiconductor, PLX, Pericom, Phoenix Contact, PMC, Qualcomm Incorporated

> CONTACT US

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