ASIC Physical Design

Learn the RTL-to-GDSII implementation flow, from inputs and floorplanning through timing closure and physical verification.

What you will study

01	**Foundations** Electronics and CMOS; digital logic; UNIX/Linux; ASIC flow; Verilog; DFT basics; Tcl scripting.
02	**Synthesis and timing** Synthesis inputs and constraints; optimization; static timing analysis and timing checks.
03	**Floorplanning and power** Input sanity checks; IO placement; floorplanning; power grid; IR drop and electromigration concepts.
04	**Implementation** Standard cell placement; congestion; clock tree synthesis; routing; signal integrity.
05	**Closure and verification** Post-route optimization; engineering change orders; timing closure; DRC, LVS and electrical checks.
06	**Practice and review** Physical design project execution and mock interview preparation.

Batch and learning format

For confirmed start dates, visit the live batch calendar. Online and Hyderabad/Bengaluru classroom options are advertised. Ask admissions to confirm the timetable, seat availability, fees and current lab access for your chosen batch.

Explore the current course page

https://chipxpert.in/asic-physical-design-course/

For admissions: +91 83098 18310 | chipxpert.in/contact/