

Advanced RTL Design

Learn synthesizable RTL design using Verilog and SystemVerilog, with microarchitecture, simulation, lint and timing-aware handoff.

What you will study

- 01 **RTL foundations**
RTL methodology, datapath versus control, synthesizable coding style and design intent.
- 02 **Microarchitecture**
Finite-state machines, pipelining, hazards and block-level architecture.
- 03 **Clock and reset**
Clock-domain crossing concepts, reset strategies and initialization.
- 04 **Quality checks**
Simulation and debug, lint, CDC checks and timing-aware constraints.
- 05 **Low power and handoff**
Clock-gating concepts, introductory UPF and a structured RTL handoff checklist.
- 06 **Practice and review**
Block-level RTL exercise with synthesis-oriented review.

Batch and learning format

For confirmed start dates, visit the [live batch calendar](#). Online and Hyderabad/Bengaluru classroom options are advertised. Ask admissions to confirm the timetable, seat availability, fees and current lab access for your chosen batch.

Explore the current course page

<https://chipxpert.in/vlsi-advanced-rtl-design-course-online-offline/>

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